A HIGH-EFFICIENCY POWER SUPPLY USING MICROLOGIC® INTEGRATED CIRCUITS *

by Sam Schwartz

I. INTRODUCTION

A design for a switching-type, high-efficiency power supply with excellent performance using integrated circuits and ultra high-speed, power output transistors is described. The largely integrated control section makes it possible to build small, compact units featuring low assembly and maintenance costs. In addition, the extremely fast turn-on and turn-off times of the output devices minimize switching dissipation so that high operating frequencies can be used and the power transformer itself therefore can be small.

Although the unit built at Fairchild Semiconductor provides a DC output of +20 V, the design can easily be adapted to supply almost any output voltage desired—for example, 3.5 V for μL^{TM} integrated circuit elements in an airborne application, or both +12 V and -6 V for transistor circuitry in a variety of other applications. The design described here uses μL elements that operate in the industrial and commercial temperature range; however, components for military environments suggested in Tables I and II can be substituted if the application requires them.

The voltage regulation for the +20 V supply is 1 percent for a load variation of 0 to 5 A, and could be improved by providing higher gain within the feedback loop.

The overall power supply includes the following units (see Fig. 1):

- Control circuitry, an integrated section which supplies symmetrical waveforms to the driver and power output stages, thus greatly facilitating transformer construction
- Driver and "high-level logic" stages, which provide power gain
- Output stage, which supplies power to the load
- Reference and error amplifier, which provides voltage regulation by feeding back an error voltage from the output to the operational amplifier in the control circuitry to adjust the conduction time of the output switching amplifiers.

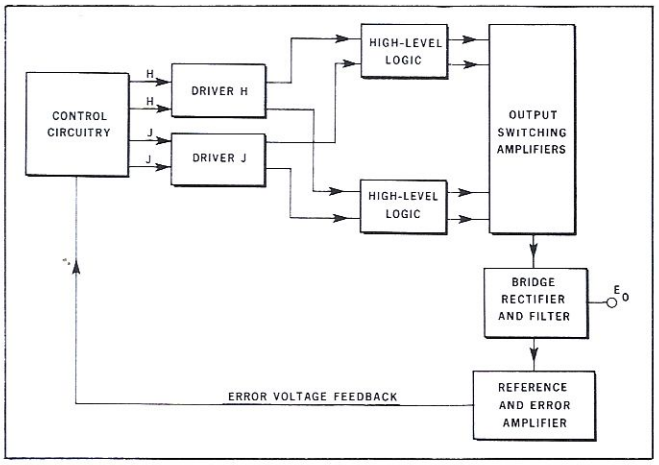

Fig. 1. Block diagram of overall power supply.

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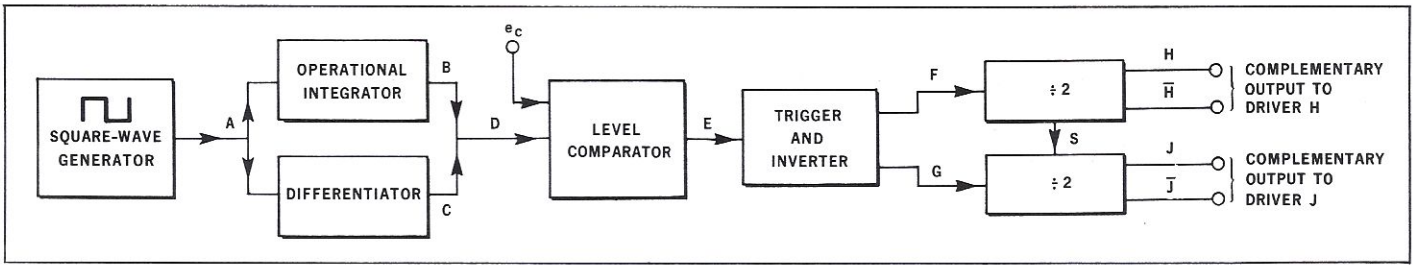


Fig. 2. Control circuitry, block diagram.

II. CONTROL CIRCUITRY

Design of the control circuitry features a unique combination of analog and digital techniques (reference should be made to Figs. 2 to 4 during the following discussion). The square wave generator output (A) is separately integrated and differentiated, producing waveforms B and C, whose sum (D) is a triangular peaked waveform appearing at one input to the level comparator, while a steady error or control voltage, e_C, appears at the other. Twice per cycle, the instantaneous value of waveform D passes above or below e_C and causes the comparator output to change level, forming a square wave. If the level of e_C shifts up or down, the leading and trailing edges of the output square wave shift about the peaks of the triangular wave, and symmetry is thus preserved. The positive- and negative-going spikes on waveform D prevent an inoperative condition when e_C becomes larger or smaller than the peak values of the triangular wave alone.

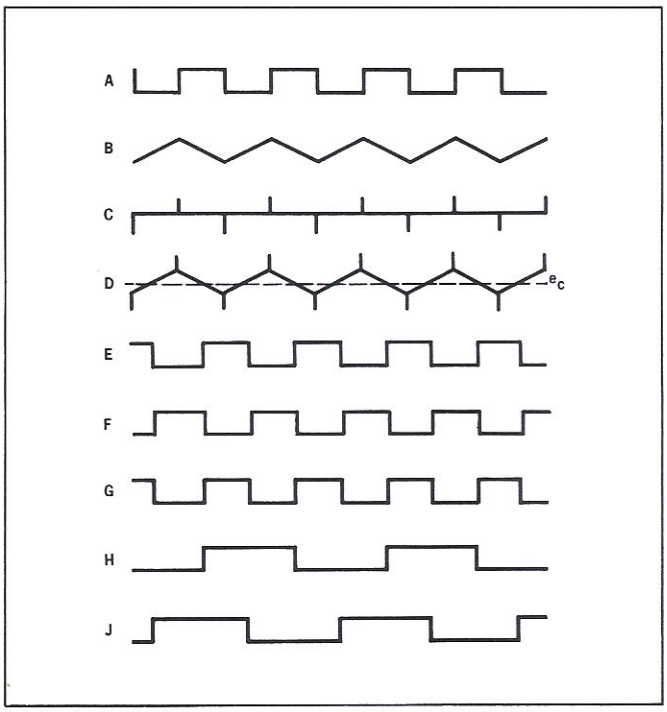


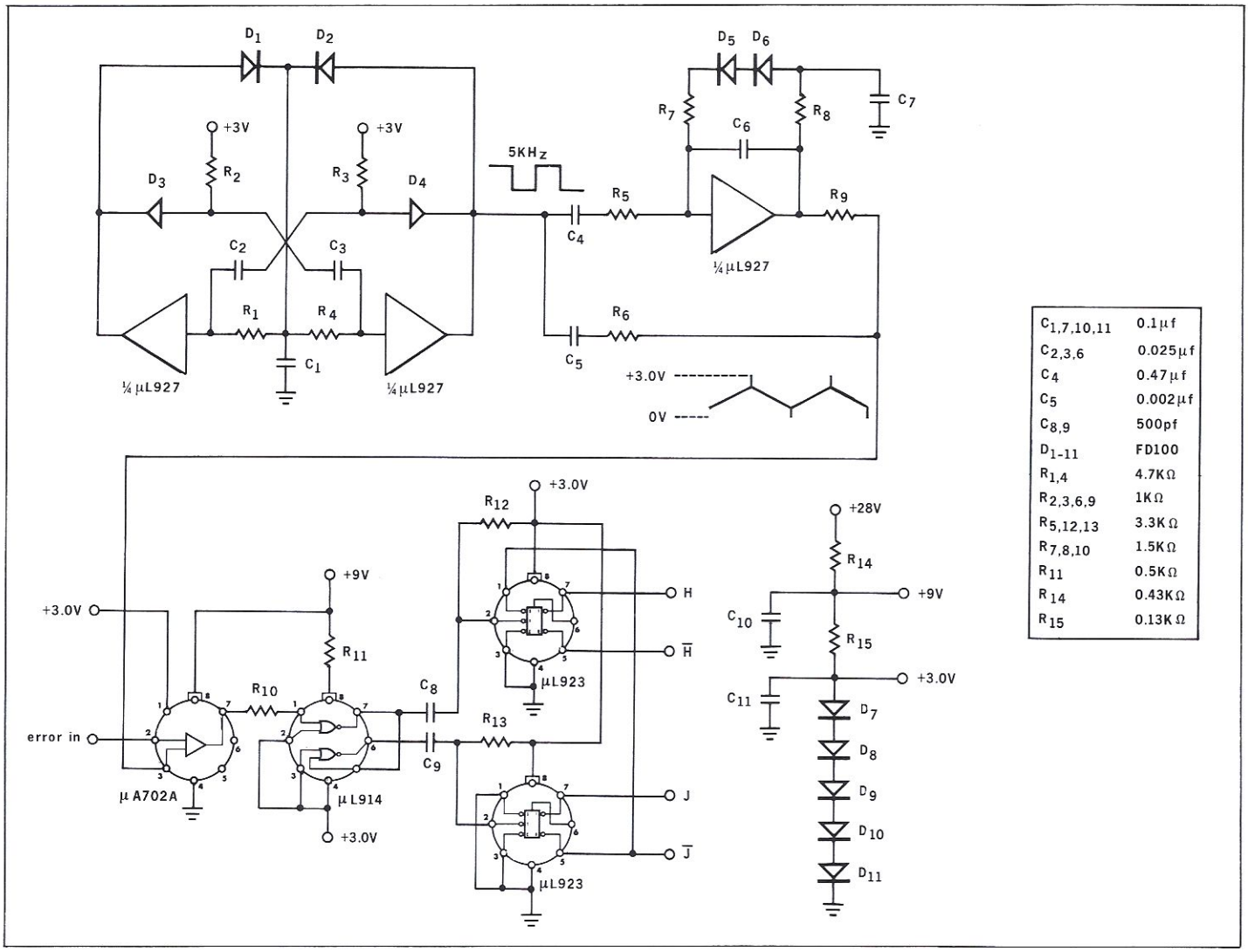
Fig. 3. Control circuitry, waveforms.

The trigger and inverter circuit decreases the rise time of the comparator square wave and produces complementary waveforms (F and G) to drive the binaries, whose outputs are directly coupled to the associated driver circuits. To prevent a 180-degree phase ambiguity that could otherwise occur in the binary outputs when DC supply power is first applied, the binaries are interconnected so that the state of one controls the state of the other. Each binary puts out a pair of complementary square waves (H, $\overline{H}$, and J, $\overline{J}$), whose frequency is half that of the square-wave generator output.

Square-wave Generator

The square-wave generator is a self-starting symmetrical multivibrator composed of two of the gates in a μL 927 quad inverter. Its frequency (5 kHz) is controlled by the equal-time-constant pairs, R_1C_2 and R_4C_3. Proper initiation and maintenance of multivibrator action is ensured in the following manner: The collector of each μL 927 inverter is connected through a diode (D_1 or D_2) to capacitor C_1, which supplies drive to the bases of both inverters. Diodes D_1 and D_2 form a logical "OR" gate that allows capacitor C_1 to become charged if either or both outputs from the inverter collectors go in the positive direction. Thus, it is impossible for both inverters to be saturated simultaneously, a condition that would eliminate both base drives. After the multivibrator is running normally, the required charge on C_1 is maintained by alternate conduction of D_1 and D_2.

To ensure a square-wave output of approximately equal rise and fall times, the collector of each inverter is returned to the supply voltage not only through the discrete components D_3R_2 and D_4R_3, respectively, but also through an integrated resistor inside the Microloigc® element. By taking the output put across this integrated resistor, the usual degradation of rise time due to charging current from the coupling capacitor (C_2 or C_3) is avoided because this current flows through the discrete-component resistor and is isolated from the output by the diode (D_3 or D_4). Although only one output is required,



$C_{1,7,10,11}$	0.1µf
$C_{2,3,6}$	0.025µf
C_4	0.47µf
C_5	0.002µf
$C_{8,9}$	500pf
D_{1-11}	FD100
$R_{1,4}$	4.7KΩ
$R_{2,3,6,9}$	1KΩ
$R_{5,12,13}$	3.3KΩ
$R_{7,8,10}$	1.5KΩ
R_{11}	0.5KΩ
R_{14}	0.43KΩ
R_{15}	0.13KΩ

Fig. 4. Control circuitry, schematic diagram.

the external path to the supply voltage is added to both collectors to help maintain symmetry of output.

Operational Integrator

The operational integrator consists of capacitor C_6 resistor R_5, and one gate in the µL927 element connected as a single stage inverting amplifier appropriately biased for Class-A operation. Forward-biased diodes D_5 and D_6 provide self-regulating Class-A bias similar to the conventional zener-biasing method but more suited to this circuit because of the low voltage bias requirement. Emitter-resistor bias could not be used in view of the low supply voltage (3 V DC). Base bias current is obtained from the collector circuit through the bias diodes and through resistors R_7 and R_8. A DC collector voltage of about one-half the supply, or 1.5 V, is fixed primarily by the V_{BE} of the µL927 transistor and the two diode drops, the voltage dropped across R_7 and R_8 being small. Capacitor C_7 and resistor R_8 form a low-pass filter that couples the DC component of the collector voltage to the bias diodes. Since the integrator operates only on an AC basis, integrating a symmetrical square wave, coupling capacitor C_4 simplifies coupling between the square-wave generator and the integrator by blocking DC voltage.

Differentiator

The differentiator circuit consists of capacitor C_5 and resistors R_6 and R_9. Because the output of the integrator is introduced at one end of R_9, current summing of the integrated and differentiated waves produces the previously described triangular peaked waveform at the junction of R_6 and R_9. This waveform is directly coupled into one input of the level comparator, and the controlling error voltage is introduced into the other.

Level Comparator

The level comparator is a μA 702A analog integrated element operating without feedback. The effect of the DC component of the direct-coupled triangular wave is offset by biasing the operational amplifier in the following manner: pin 4 of the μA 702A, which is normally connected to a negative supply, is grounded; pin 1, the common amplifier input terminal, is operated at +3 V DC, and the positive-supply input terminal, pin 8, at +9 V. Thus, the effective positive and negative supply voltages are +6 V and -3 V, and a single output (a square wave of controlled duration) is taken from pin 7.

Trigger and Inverter

A μL 914 dual 2-input gate, connected as a cascaded pair of saturating amplifiers between the comparator and the frequency dividers, serves two functions:

- Decrease the rise and fall times of the square wave
- Provide complementary inputs to the dividers

Frequency Divider

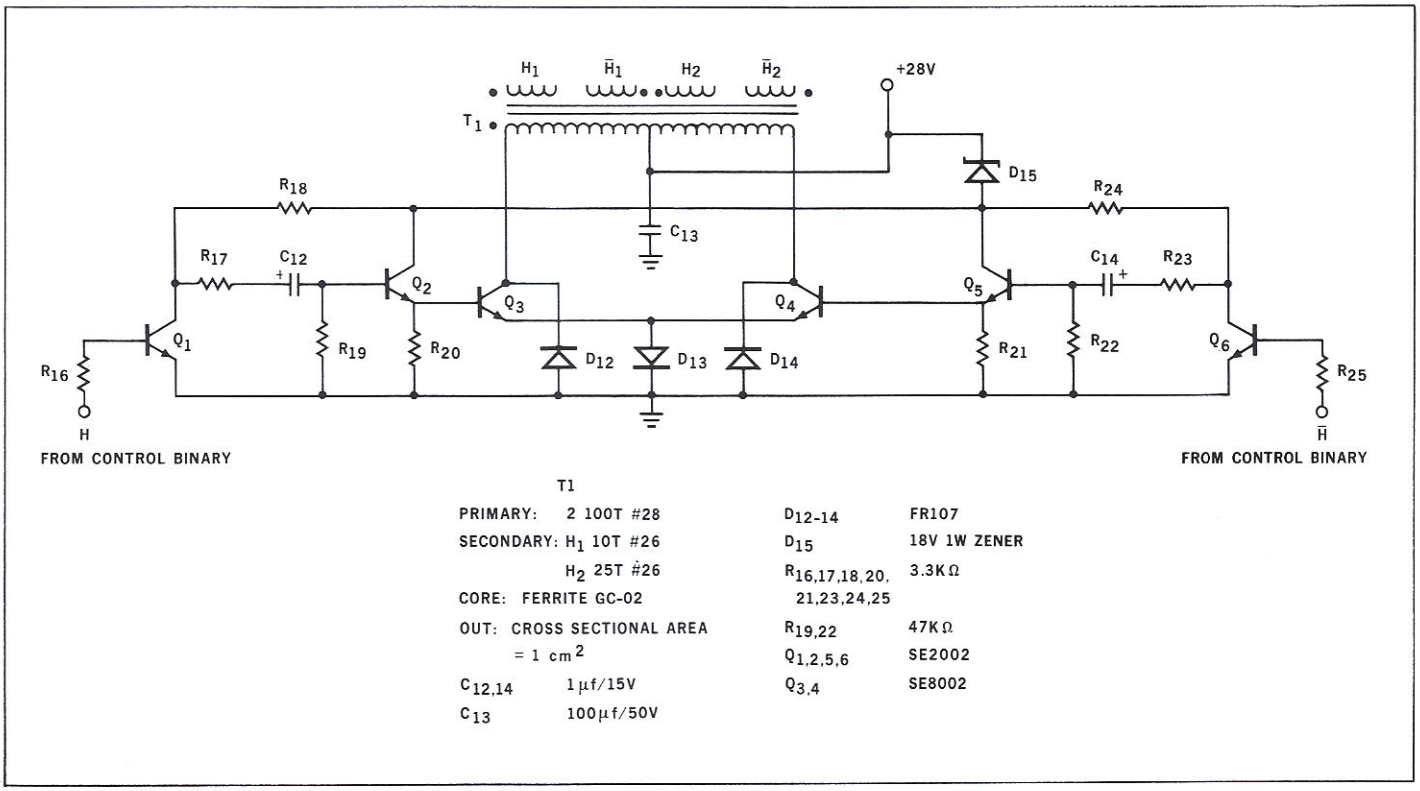
Two μL 923 J-K flip-flop elements divide the input trigger pulses by two, providing complementary, symmetrical outputs displaced from each other in time by the width of the input pulse. Suitable negative-going pulses for the trigger (pin 2) input of each divider are obtained by coupling and differentiating the complementary square wave outputs from the μL 914 gates through networks C_8R_{12} and C_9R_{13}, respectively. The ambiguity-elimination set line goes from pin 5 of the lower binary to pin 1 of the upper. Complementary outputs are obtained from pins 5 and 7 of each binary.

Supply Voltage

The required supply potentials are obtained from the combination resistor-diode divider network consisting of resistors R_{14} and R_{15} and diodes D_7 through D_{11}. Appropriate points are bypassed by capacitors C_{10} and C_{11}.

III. DRIVER CIRCUITRY

The driver circuitry features push-pull operation, each device conducting a full 180 degrees. A single driver circuit ("H") is shown schematically in Fig. 5. The driver power-output transistors, Q_3 and Q_4, are predriven by Q_2 and Q_5. Since the one-volt level of the symmetrical, complementary drive voltage signals (H and $\overline{H}$) from the control binaries is insufficient to control predrivers Q_2 and Q_5 directly, voltage-gain stages Q_1 and Q_6 are added. Capacitive coupling is used between the collectors of the voltage-gain stages and the bases of the predrivers. In the absence of drive signals, transistors Q_2 and Q_5, being unbiased, will not conduct, thus eliminating the danger of



T1

PRIMARY:	2 100T #28
SECONDARY:	H_1 10T #26
	H_2 25T #26
CORE:	FERRITE GC-02
OUT:	CROSS SECTIONAL AREA = 1 cm^2
$C_{12,14}$	1 μf/15V
C_{13}	100 μf/50V

D_{12-14}	FR107
D_{15}	18V 1W ZENER
$R_{16,17,18,20,21,23,24,25}$	3.3K Ω
$R_{19,22}$	47K Ω
$Q_{1,2,5,6}$	SE2002
$Q_{3,4}$	SE8002

Fig. 5. Schematic diagram of driver H.

overdissipation of output transistors Q_3 and Q_4. To provide further assurance of turn-off in the absence of drive, diode D_{13} is placed in the common-emitter path of both output devices. Direct coupling may be used between the control binaries and the voltage-gain stages to minimize components.

The predriver stages are in the common-collector configuration, directly coupled into the bases of output transistors Q_3 and Q_4. The predriver collectors are supplied with +10 V DC through zener diode D_{15}. The output-transistor bases are referenced to ground by resistors R_{20} and R_{21}. Diodes D_{12} and D_{14}, used for transient damping, return the energy stored in the leakage inductance of the driver output transformer, T_1, to the power supply. Capacitor C_{13} is a supply bypass.

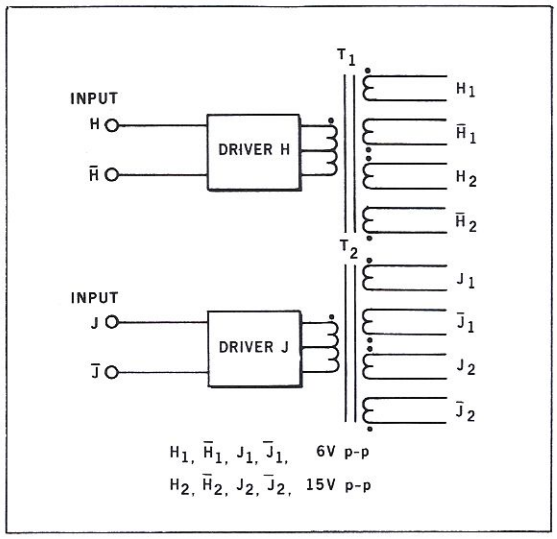


Fig. 6. Driver transformers.

IV. HIGH-LEVEL LOGIC CIRCUITRY

Two secondary windings of each driver transformer supply 6 V peak to peak, and two supply 15 V peak to peak (see Fig. 6). The secondary windings are connected to the high-level logic circuits (see Fig. 7), which supply symmetrical, positive-going pulses (waveform ⑤ in Fig. 8) to the output switching devices.

Turn-off Waveform

Waveform ③ in Fig. 8 is generated by combining $\bar{H}_2$ and J_2 in a logical OR gate. When either $\bar{H}_2$ or J_2 is negative, ③ is negative; otherwise it is zero. Diodes D_{16} and D_{17} (Fig. 7) assure that only a negative-going output will appear at ③. Capacitor C_{15} determines the charge initially removed from the output transistor base to effect turn-off, and resistor R_{26} serves two functions:

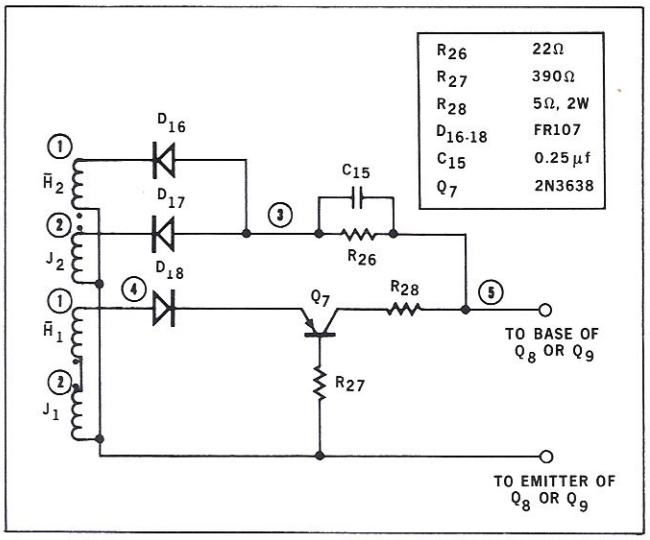


Fig. 7. High-level logic circuitry.

- To provide a direct path to the output transistor base to maintain cutoff
- To supply a discharge path for C_{15} so that this capacitor will be ready to absorb charge on its next operating cycle

Note that waveform ⑤ at the output transistor base is alternately negative for turn-off and positive for turn-on.

Turn-on Waveform

When $\bar{H}_1$ and J_1 are of the same polarity, waveform ④ is of this polarity, but when $\bar{H}_1$ and J_1 are of opposite polarity, no voltage appears at ④. The magnitude of ④ is the linear sum of $\bar{H}_1$ and J_1. During the turn-on interval, D_{18} is forward-biased and the base drive applied to Q_7 through R_{27} is negative, so that Q_7 is driven into saturation. Thus a path exists to the output transistor base ⑤ for a turn-on current whose magnitude is limited by R_{28}.

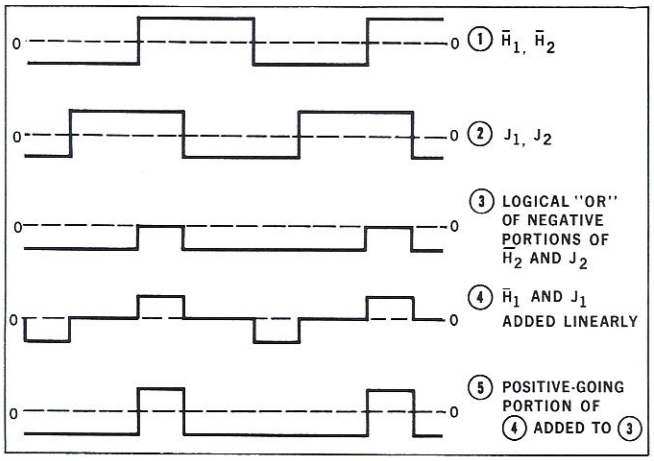

① H̄1, H̄2
② J1, J2
③ LOGICAL "OR" OF NEGATIVE PORTIONS OF H̄2 AND J2
④ H̄1 AND J1 ADDED LINEARLY
⑤ POSITIVE-GOING PORTION OF ④ ADDED TO ③

Fig. 8. Waveforms, driver transformer and high-level logic circuitry.

Isolation

Isolation between the turn-on and turn-off circuits is provided as follows: During the turn-off interval when $\bar{H}$ and J are negative, D_{18} is reverse-biased and Q_7 is held off by the positive signal on its base. Thus no path for current flow from point (3) to point (4) exists. During the turn-on interval, when $\bar{H}$ and J are positive, $\bar{H}_2$ and J_2 are of larger amplitude than $\bar{H}_1$ and J_1. Current flow is therefore prevented by reverse bias on diodes D_{16} and D_{17}.

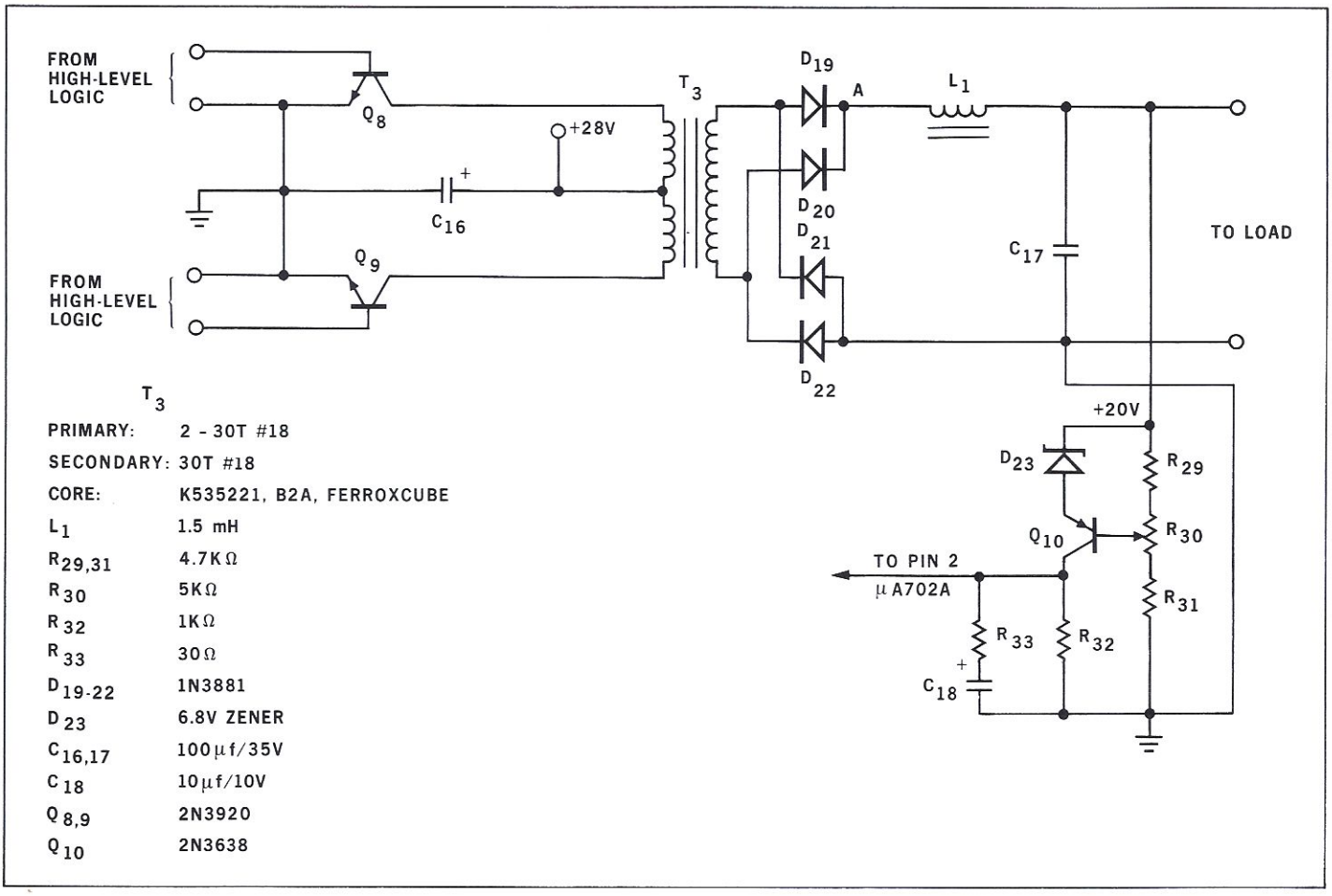
V. OUTPUT STAGE

The output stage consists of two switching power amplifiers, Q_8 and Q_9, transformer-coupled to the rectifier and filter circuitry (see Fig. 9). This stage supplies power to the load, and voltage to a reference amplifier (Q_{10}) for voltage regulation. Transistors Q_8 and Q_9 are arranged in a push-pull configuration and held alternately on and off by positive- and negative-going signals from the high-level logic circuitry. Capacitor C_{16} bypasses the power input terminal and provides a low-impedance path to ground for the load current. Coupling transformer T_3 operates as a linear transformer. A bridge (diodes D_{19}, D_{20}, D_{21}, and D_{22}) is used to rectify the output. Alternatively, a full-wave rectifier could be used with a center-tapped secondary on the transformer, which would be somewhat more difficult to construct.

The rectified square wave from the bridge, filtered by L_1 and C_{17}, supplies a constant DC voltage to the load. The necessary excitation current for L_1 is normally supplied through the load; for operation without external load, therefore, a small resistor (about 100 Ω) is shunted across the output terminals.

VI. REFERENCE AND ERROR AMPLIFIER

Voltage regulation is provided by the error amplifier and voltage reference, consisting of Q_{10} and zener diode D_{23} (see Fig. 9). This unit feeds back an error voltage to the μA 702A comparator to adjust the duty cycle of the output square wave from the control circuitry.



T_3	
PRIMARY:	2 - 30T #18
SECONDARY:	30T #18
CORE:	K535221, B2A, FERROXCUBE
L_1	1.5 mH
$R_{29,31}$	4.7KΩ
R_{30}	5KΩ
R_{32}	1KΩ
R_{33}	30Ω
$D_{19\text{-}22}$	1N3881
D_{23}	6.8V ZENER
$C_{16,17}$	100μf/35V
C_{18}	10μf/10V
$Q_{8,9}$	2N3920
Q_{10}	2N3638

Fig. 9. Schematic diagram of output stage and reference and error amplifier.

The action of the regulator is as follows: If, for example, the line voltage or the load voltage increases, the corresponding increase in output voltage appears at the emitter of Q_{10} as well as across the voltage divider network, R_{29}, R_{30}, and R_{31}. Since less of the increase appears at the base of Q_{10} than at its emitter, Q_{10} conducts more heavily, so that its collector voltage—and therefore the error voltage to the μA 702A comparator—rises. As explained in the section on control circuitry, an increase in error voltage causes a decrease in duty cycle of the output square wave and consequently a decrease in the rectified DC voltage across filter capacitor C_{17} in the output.

The same mechanism can be used to change the load voltage by adjusting the potentiometer at the base of Q_{10}. Moving it up, for example, causes the base of Q_{10} to go more positive than its emitter, so that transistor conduction decreases and the error voltage decreases, increasing the duty cycle of the output waveform from the switching amplifiers and thus increasing the load voltage.

For variation in load current from 0 to 5 A, the amplifier built at Fairchild supplies +20 V output with one-percent variation. The oscillograms in Fig. 10 show the variations in pulse duration of the output waveform for changes in load current at constant line voltage (left-hand column) and for changes in line voltage at constant load current (right-hand column). The upper waveform in each oscillogram is taken from the collector of one of the switching amplifiers (Q_8 or Q_9), and the lower waveform is taken across the bridge. It can be seen from these oscillograms that (1) if load current is gradually increased, with the line voltage held constant (left-hand column), the conduction time of both waveforms increases to maintain a constant output voltage; and (2) as the line voltage increases with the load current held constant, the conduction time decreases (right-hand column).

Note that the upper waveform in Oscillogram No. 1 (with zero load current) is not a perfect square wave and that small spikes occur in the upper waveforms of all the oscillograms. These distortions could be eliminated by critically damping the leakage inductance of the power transformer, T_3; however, they do not interfere with proper circuit operation, and the price for removing them would be a loss in overall efficiency due to power losses in the damping network.

The ringing in the lower waveform in Oscillogram No. 1 is due to low energy dissipation in the choke and can be explained as follows: Current flows through the filter-rectifier circuit during the entire conduction period. When the voltage across T_3 goes to zero, the energy stored in L_1 causes Point A (Fig. 9) to go sufficiently below ground to permit conduction of the bridge diodes. (This negative-going excursion is too small to appear in the oscillogram.) The period of nonconduction is so long under the no-load condition that the energy in the choke becomes insufficient to maintain diode conduction, and the remainder therefore dissipates through the internal resistance of the choke. The observed ringing is produced by exchanges of energy between the inductance and stray capacitance of the choke as the voltage at the choke input levels off to the average value across C_{17}. Ringing is not observed under load conditions for two reasons:

- At higher currents, the stored energy in the choke is sufficient to hold the diode bridge in conduction between transistor conduction intervals.
- Under load conditions, the time of transistor nonconduction is shortened by feedback action to maintain the output voltage constant.

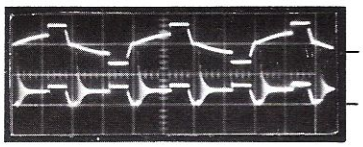
As is characteristic of a switching type of power amplifier with feedback control, this supply operates at constant efficiency over a wide range of input voltages. In other words, the input power remains essentially constant for a constant load current and voltage, any increase in line voltage being balanced by a decrease in line current. It should be noted, however, that increasing the line current causes increased power loss in the switching transistors and bridge rectifier and thus reduces the overall efficiency slightly at higher line currents.

VII. PERFORMANCE OF SUPPLY

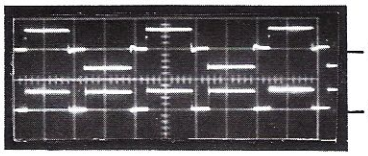
Efficiency and regulation curves for the power supply are shown in Fig. 11. The regulation characteristic in Fig. 11(a), plotted as a function of load current at a constant 30-watt input supply level, shows a one-percent variation in output voltage from no load up to 1 A. From 1 to 5 A, the output voltage remains constant. The regulation curve in Fig. 11(b) shows that the output remains constant as the input supply voltage changes from 25 to 33.5 V. The load current under this condition is a constant 2.1 A. The efficiency curve in Fig. 11(c) shows a peak efficiency of 82.5 percent at 3 A of output current. The element in the supply that contributes the largest loss is the bridge rectifier. At 5 A a single rectifier drop is 1.5 V, so that the total bridge drop, through two series rectifiers, is 3 V. If the supply requirement had necessitated a higher DC output voltage, the efficiency would have increased because of the lower diode loss at the reduced current. The efficiency curve in Fig. 11(d) shows a change in efficiency of only 2 percent as the input voltage is changed over the extreme range of 25 to 33.5 V.

CONSTANT LINE VOLTAGE

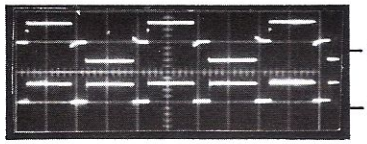
(E_{in}=30V)

1  I_{in}=0.15A

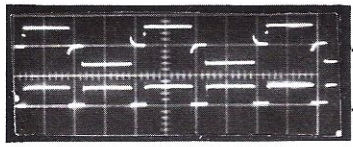
E_o=20.2V, I_o=0A

2  I_{in}=0.9A

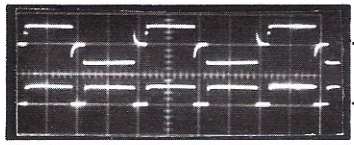
E_o=20V, I_o=1.1A

3  I_{in}=1.7A

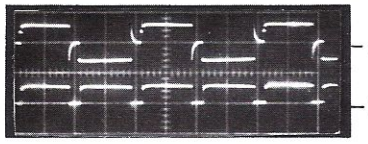
E_o=20V, I_o=2.1A

4  I_{in}=2.5A

E_o=20V, I_o=3.1A

5  I_{in}=3.35A

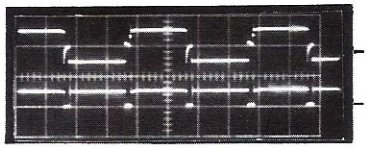
E_o=20V, I_o=4A

6  I_{in}=4.3A

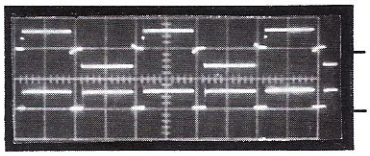
E_o=20V, I_o=5A

CONSTANT LOAD CURRENT

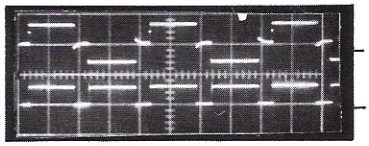
(E_o=20V, I_o=2.1A)

7 

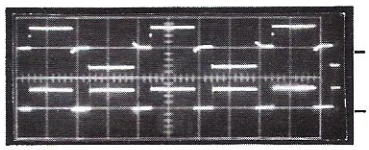
E_{in}=25V, I_{in}=2.1A

8 

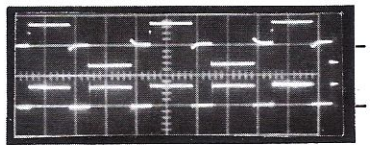
E_{in}=28V, I_{in}=1.85A

9 

E_{in}=30V, I_{in}=1.7A

10 

E_{in}=32V, I_{in}=1.62A

11 

E_{in}=33.5V, I_{in}=1.55A

SCALE

Vertical: 50V/cm

Horizontal: 50μsec/cm

Fig. 10. Oscillograms of output waveforms from switching amplifier collector (top waveform each oscillogram) and across bridge (bottom waveform).

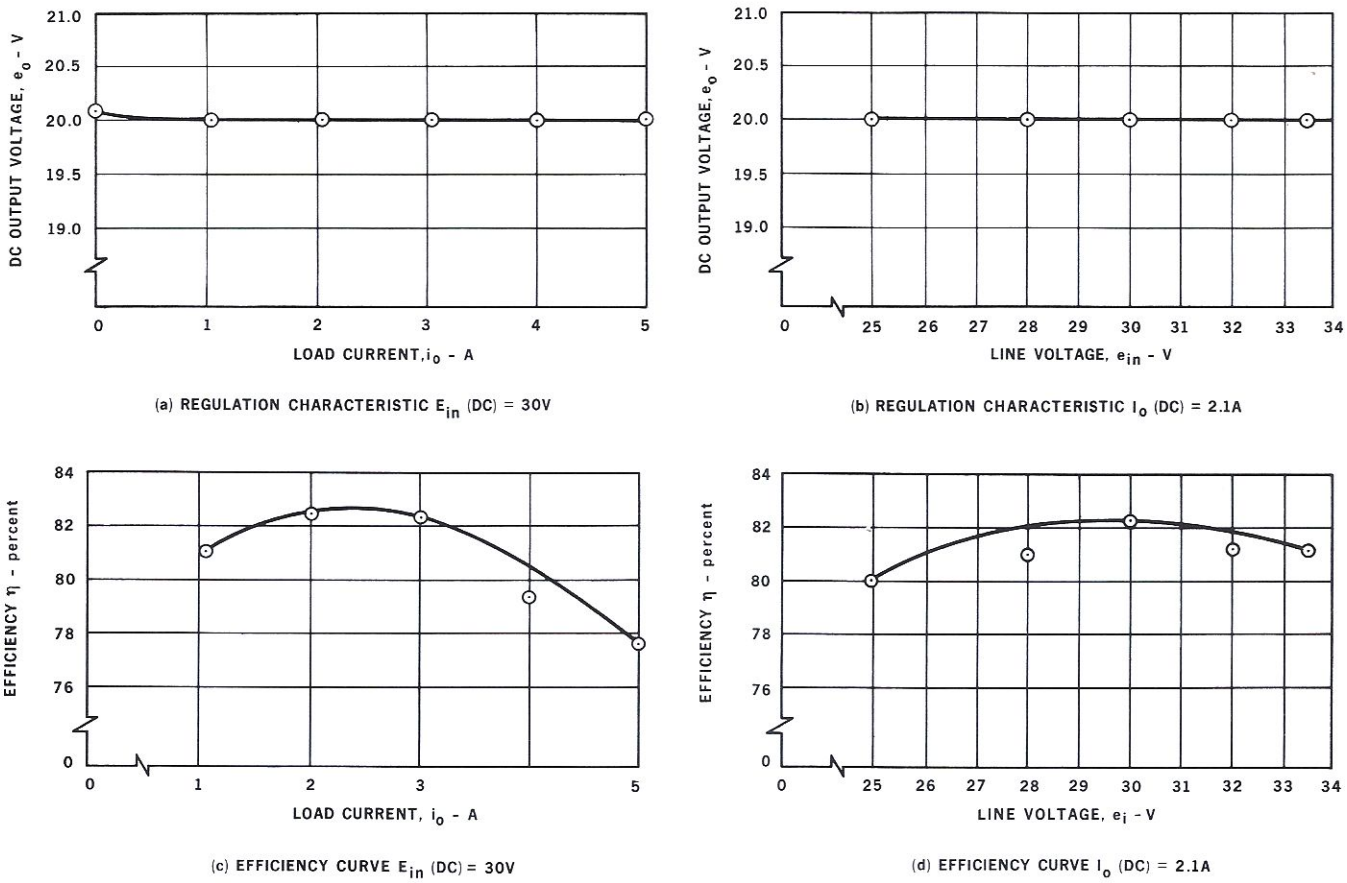


Fig. 11. Regulation and efficiency curves for power amplifier/rectifier-filter combination.

TABLE I

TRANSISTOR COMPLEMENT

Device	T_{max} (oper.)	P_{max}	h_{FE}	V_{CE}(sat)	BV_{CBO}	T_S	Remarks
SE2002 (2N916)	125°C	0.3 W at 65°C case	100 - 400 I_C = 10 mA V_{CE} = 1 V	0.7 V I_C = 10 mA I_B = 1 mA	35 V I_C = 0.1 mA I_E = 0	—	General-purpose NPN with low V_{CE}(sat)
SE8002 (2N3110)	200°C	2.8 W at 100°C case	40 - 120 I_C = 150 mA V_{CE} = 1 V	1.2 V I_C = 1.0 A I_B = 0.1 A	80 V I_C = 100 μA I_E = 0	—	Medium-power NPN with low V_{CE}(sat)
2N3638	125°C	0.42 W at 65°C case	30 - 67 I_C = 50 mA V_{CE} = -1 V	-0.25 V I_C = 50 mA I_B = 2.5 mA	-25 V I_C = 100 μA I_E = 0	—	Medium-high-current PNP switch
2N3920	150°C	15 W at 75°C	100 - 300 I_C = 2 A V_{CE} = 2 V	1.2 V I_C = 10 A I_B = 1 A	12.0 V I_C = 5 mA I_E = 0	t_{on} = 0.5 μsec t_{off} = 1 μsec I_C = 10 A	High-current NPN switch

TABLE II

DIODE COMPLEMENT

Device	BV	I_R	V_F	t_{rr}	P_D	Package	Remarks
FD-100 (1N3064)	≥75 V I_R = 5 μA	≤100 nA V_R = 50 V	≤1 V I_F = 10 mA	≤4.0 nsec I_F = I_R = 10 mA, rec. to 1.0 mA	≥250 mW	DO-7 glass*	High-speed switch
FR-107	≥250 V I_R = 500 μA	≤500 nA V_R = 150 V	≤1 V I_F = 1.0 A	≤100 nsec I_F = 1.0 A V_R = 30 V	≥1.0 W	1 W glass	High-speed rectifier

*FDM1000 low-cost epoxy unit can be used in commercial and industrial applications (T_A <125°C).